TEAC FD-235HF-4217
MICRO FLOPPY DISK DRIVE
SPECIFICATION

1. OUTLINE

This specification provides a description for the TEAC FD-235HF, double sided, dual density, 3.5 inch floppy disk drive (hereinafter referred to as the FDD). Table 1 shows the outline of the FDD.

Model name	FD-235HF-4217	
Safety standard on label	UL & CSA	
Operation modes	High density mode, Write and read	Normal density mode, Write and read
3.5" disk used	High density (2HD)	Normal density (2DD)
Unformatted data capacity	2M bytes	1M bytes
Data transfer rate	500k bits/sec	250k bits/sec
Disk rotational speed	300rpm	
Track density	135tpi	
Track to track time	3msec	
Required power	+5V single (4.5 ~ 5.5V)	
Front bezel & flap	Beidge (AT)	
Eject button	Beidge (AT)	
LED indicator color	Amber	
Density mode designation	Customer selection among several methods, refer to items 8.3.13 and 11.	
Signal output driver	Open collector TTL	
Input signal terminator	1kΩ ± 5%, unremovable	
Customer selectable strap	6 selections, refer to item 11.1.	
Function setting at delivery	1. Strap setting 1.1 DS1: DRIVE SELECT 1 on pin 12 1.2 HA: Automatic density setting by HD hole (Interface pin 2 is OPEN.) 2. Other function setting 2.1 LED turn-on condition: DRIVE SELECT 2.2 Motor rotating condition: MOTOR ON 2.3 Ready and seek-complete gate (full-mask) for INDEX and READ DATA output pulses 2.4 DISK CHANGE on pin 34 2.5 Auto-chucking, auto-recalibration 2.6 FDD frame is electrically shorted to DC 0V.	
Interface connector	34 pin right angle header connector and power connector	
Other optional function	Not equipped.	

(Table 1) Specification outline

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The FDD is equipped with a discrimination switch for the high density (HD) hole of a disk cartridge and customer selectable straps for designating method of the density mode. Refer to item 11 as to the detailed explanation.

When a high density disk is installed and the high density mode is designated, the FDD operates at 2MB mode, while it operates like conventional 1MB FDD when a normal density disk is installed and 1MB mode is designated.

2. DISK

3.5" micro floppy disks which are mutually agreed between the customer and TEAC.

For 1MB mode: Normal density disk (2DD)
2MB mode: High density disk (2HD)

3. PHYSICAL SPECIFICATION

(1) Width: 101.6mm (4.00 in), Max.

(2) Height: 25.4mm (1.00 in), Nom.

(3) Depth: 145mm (5.71 in), Max., excluding front bezel

(4) Weight: 350g (0.77 lbs), Nom., 370g (0.82 lbs), Max.

(5) External view: See Fig.1.

(6) Cooling: Natural air cooling

(7) Mounting: Mounting for the following directions are acceptable.

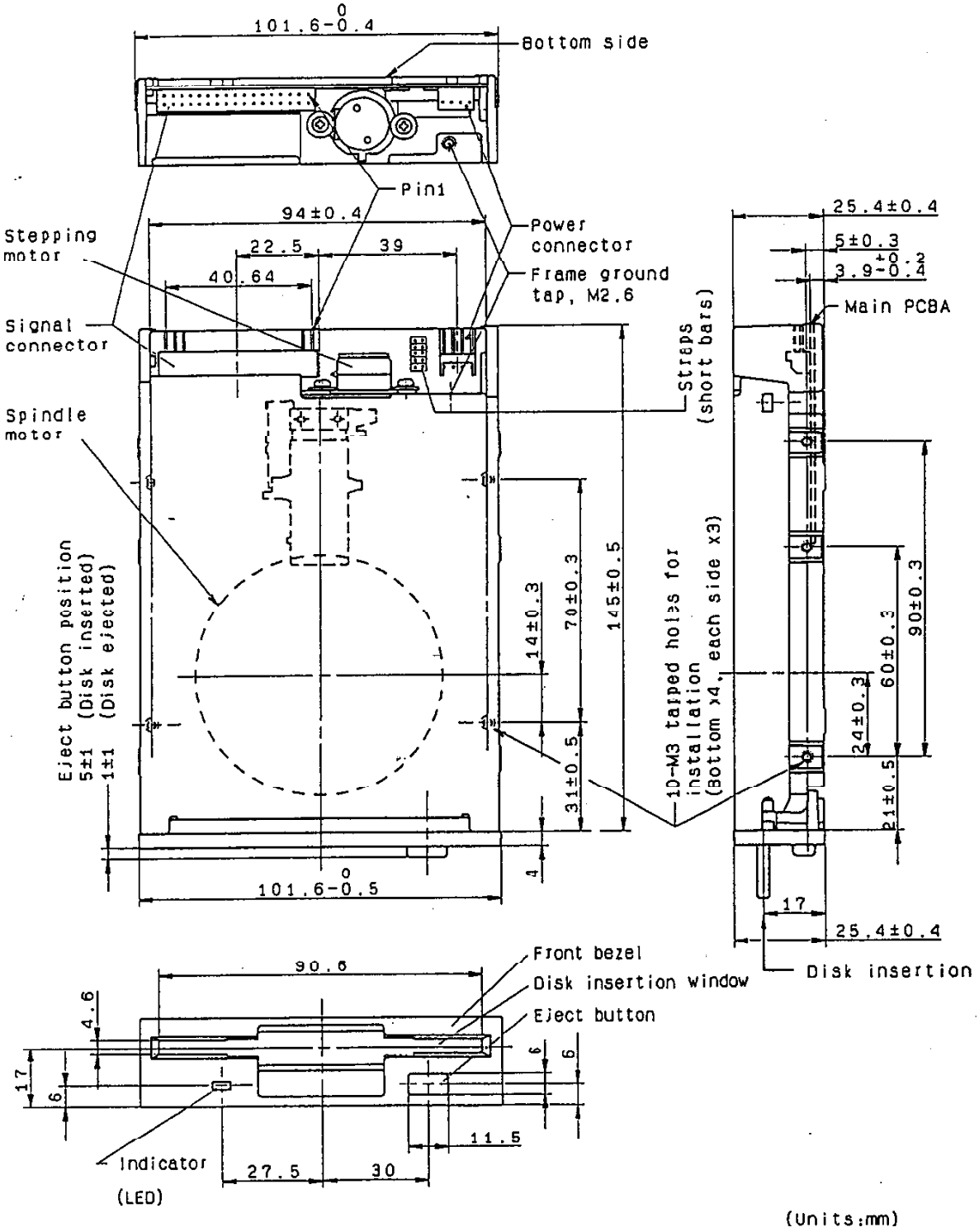
(a) Front loading, mounted vertically.
(b) Front loading, mounted horizontally with spindle motor down.
(c) Mounting angle in items (a) and (b) should be less than 25° with front bezel up or down.

Note: As to the other mounting directions than the above will be considered separately.

(8) Installation: With installation holes on the frame of the FDD. Refer to Fig.1.

(9) Material of frame: Aluminum diecast

(10) Material of front bezel: PPHOX (Xyron, complying with UL94-5V)



(Fig.1) FDD external view

4. OPERATIONAL CHARACTERISTICS

4.1 2MB Mode Data Capacity

Recording method				FM	MFM
Data transfer rate (k bits/sec)				250	500
Tracks/disk				160	160
Innermost track bit density (bpi)				8,717	17,434
Innermost track flux density (frpi)				17,434	17,434
Data capacity	Unformatted		k bytes/track	6.25	12.50
			k bytes/disk	1,000	2,000
	Formatted	32 sectors /track	k bytes/sector	0.128	0.256
			k bytes/track	4.096	8.192
			k bytes/disk	655.36	1,310.72
		18 sectors /track	k bytes/sector	0.256	0.512
			k bytes/track	4.608	9.216
			k bytes/disk	737.28	1,474.56
		10 sectors /track	k bytes/sector	0.512	1.024
			k bytes/track	5.12	10.24
			k bytes/disk	819.20	1,638.40

(Table 2-1) 2MB mode data capacity

4.2 1MB Mode Data Capacity

Recording method				FM	MFM
Data transfer rate (k bits/sec)				125	250
Tracks/disk				160	160
Innermost track bit density (bpi)				4,359	8,717
Innermost track flux density (frpi)				8,717	8,717
Data capacity	Unformatted		k bytes/track	3.125	6.250
			k bytes/disk	500	1,000
	Formatted	16 sectors /track	k bytes/sector	0.128	0.256
			k bytes/track	2.048	4.096
			k bytes/disk	327.68	655.36
		9 sectors /track	k bytes/sector	0.256	0.512
			k bytes/track	2.304	4.608
			k bytes/disk	368.64	737.28
		5 sectors /track	k bytes/sector	0.512	1.024
			k bytes/track	2.560	5.120
			k bytes/disk	409.60	819.20

(Table 2-2) 1MB mode data capacity

4.3 Disk Rotation Mechanism

(1) Spindle motor: DC brushless motor
(2) Spindle speed: 300rpm
(3) Motor servo method: Frequency servo by ceramic oscillator
(4) Motor/spindle connection: Motor shaft direct
(5) Disk speed: 300rpm
    Long term speed variation (LSV): ±1.5% or less
    Instantaneous speed variation (ISV): ±2% or less
(6) Start time: 480msec or less
(7) Average latency: 100msec

4.4 Index Detection

(1) Number of index: 1 per disk revolution
(2) Detection method: Rotor detection of spindle motor by Hall-element
(3) Detection cycle: 197 ~ 203msec
(4) Index burst detection timing error: ±400μsec or less, with specified test disk

4.5 Track Construction

(1) Track density: 135tpi (track pitch 187.5μm)
(2) Number of cylinders: 80 cylinders
(3) Number of tracks: 80 tracks/surface, 160 tracks/disk
(4) Outermost track radius (track 00): Side 0 39.500mm (1.5551 in)
    Side 1 38.000mm (1.4961 in)
(5) Innermost track radius (track 79): Side 0 24.6875mm (0.9719 in)
    Side 1 23.1875mm (0.9129 in)
(6) Positioning accuracy: ±15μm or less, with specified test disk (Track 40, 23 ± 2°C , 45 ~ 55%RH, horizontal)

4.6 Magnetic Head

(1) Magnetic head: Read/write head with erase gap, 2 sets

(2) Effective track width after trim erase:
0.115 ± 0.008mm (0.0045 ± 0.0003 in)

(3) Read/write gap azimuth error: 0° ±18', with specified test disk

4.7 Track Seek Mechanism

(1) Head positioning mechanism: Stepping motor and lead screw
(2) Stepping motor: 4-phase, 20 steps per revolution
(3) Stepping motor drive: 2 steps per track
(4) Track 00 detection method: Photo-interrupter
(5) Track to track time: 3msec (excludes settling time, refer to item 8.3.4)
(6) Settling time: 15msec or less (excludes track to track time)
(7) Average track seek time: 94msec (includes settling time)

4.8 Window Margin and Others

(1) Window Margin (with specified test disk, MFM method, PLO separator)
2MB mode: 300nsec or more
1MB mode: 600nsec or more
(2) Recommendable write pre-compensation
Track 00 ~ 43, 2MB and 1MB modes: ±62.5 ~ ±125nsec
Track 44 ~ 79, 2MB and 1MB modes: ±125nsec
(3) Head load mechanism: Not equipped
(The FDD becomes head load condition whenever a disk is installed.)
(4) File protect mechanism: Detection of write inhibit hole by switch
(5) Disk detection mechanism: Detection of disk installation by switch
(6) Disk inserting force: 700gf or less at the center of a disk
(7) Disk ejecting force: 1,400gf or less
(8) Acoustic noise at 50cm: 50dBA or less at 3msec or 4msec seek operation
(9) Disk type descriminating mechanism: Detection of HD hole by switch
(10) Auto-recalibration: Automatic recalibration to track 00 is executed immediately after power-on.

5. ENVIRONMENTAL CONDITIONS

Note: The following requirements are applied for the unpackaged FDD.

(1) Ambient temperature
  (a) Operating : 4 ~ 51.7°C (39 ~ 125°F)
  (b) Storage : -22 ~ 60°C (-8 ~ 140°F)
  (c) Transportation: -40 ~ 65°C (-40 ~ 149°F)

(2) Temperature gradient
  (a) Operating : 20°C (36°F) or less per hour
  (b) Storage and transportation
  : 30°C (54°F) or less per hour

(3) Relative humidity
  (a) Operating : 20 ~ 80% (no condensation)
  Max. wet bulb temperature shall be 29.4°C (85°F)
  (b) Storage : 5 ~ 90% (no condensation)
  Max. wet bulb temperature shall be 40°C (104°F)
  (c) Transportation: 5 ~ 95% (no condensation)
  Max. wet bulb temperature shall be 45°C (113°F)

(4) Vibration
  (a) Operating : 1.5G or less (10 ~ 100Hz, 1oct/min. sweep rate)
  1.0G or less (100 ~ 200Hz, 1oct/min. sweep rate)
  0.5G or less (200 ~ 600Hz, 1oct/min. sweep rate)
  (b) Transportation: 2G or less (10 ~ 100Hz, 1/4oct/min. sweep rate)

(5) Shock
  (a) Operating
  Write & read: 5G (11msec, 1/2 sine wave) or less
  Read only : 10G (11msec, 1/2 sine wave) or less
  Soft errors are allowed if they are recoverable within three retries.
  (b) Transportation: 70G (11msec, 1/2 sine wave) or less

(6) Altitude (operating): -300m (-980 feet) ~ 5,000m (16,400 feet)

6. RELIABILITY

(1) MTBF: 30,000 power on hours or more (for typical operation duty)

(2) MTTR: 30 minutes

(3) Design component life: 5 years

(4) Disk life: 3×10^6 passes/track or more

(5) Disk insertion: 3×10^4 times or more

(6) Seek operation life: 1×10^7 random seeks or more

(7) Preventive maintenance: Not required (for typical operation duty)

(8) Error rate

(a) Soft error: 1 or less per 10^9 bits read
A soft (recoverable) error is defined that it can be read correctly within three retries.

(b) Hard error: 1 or less per 10^{12} bits read
A hard (unrecoverable) error is defined that it cannot be read correctly within three retries. However, it is recommended to be followed by a recalibration to track 00 and four additional retries.

(c) Seek error: 1 or less per 10^6 seeks.
A seek error is defined that it can seek to a target track within one retry including a recalibration to track 00.

(9) Safety standard: Complying with UL and CSA

(10) Electro-static discharge test: 15kv (150pF, 330Ω) or more
No hard error and/or no component damage occur when the test is applied to the operator access area (front bezel area).

7. POWER INTERFACE

7.1 Required Power

The following specifications are applied at interface connector of the FDD.

(1) DC +12V: Not required

(2) DC +5V

(a) Voltage tolerance: ±10% (4.5 ~ 5.5V)

(b) Allowable ripple voltage: 100mVp-p or less (including spike noise)

(c) Current and power consumption

Operating mode		Average current		Average power	
		Typ.	Max.	Typ.	Max.
Stand-by		3.0mA	5.0mA	15mW	28mW
Read operation		0.28A	0.38A	1.40W	2.09W
Write operation		0.28A	0.38A	1.40W	2.09W
Seek operation	3ms	0.46A	0.56A	2.30W	3.08W
	6ms	0.54A	0.66A	2.70W	3.63W
Spindle motor start		0.62A	0.70A	3.10W	3.85W

Notes:

1. Values of Typ. current and power are specified at 5.0V, while the values of Max. are at 5.5V (+10%) with a disk of large running torque.
2. Stand-by mode is defined at the stop condition of spindle motor and seek operation.
3. Rush current flows within 350msec after the motor start.
4. Short time peak current except for power-on surge is less than 0.9A.
5. Refer to item 9.4 as to the current consumption profile.

(Table 3) Current and power consumption

7.2 Power Interface Connector and Cable

(1) Power interface connector

(a) FDD side connector: AMP, P/N 171826-4 (natural color)
or equivalent

(b) Pin numbers: 4 pins

(c) Protection method for mis-connection
: Mechanical protection by the shape of connector housing

(d) Connector external view: See Fig.2.

(e) Connector location: See Fig.1.

(f) Power interface connections: See Table 4.

(g) Cable side matched connector: AMP P/N 171822-4 (natural color)
or equivalent

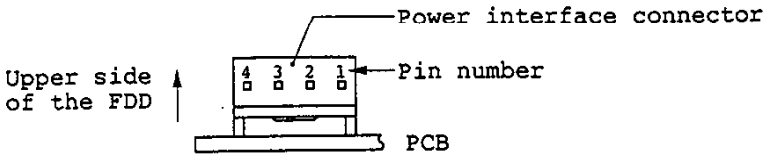
(h) Cable side matched pin: AMP P/N 170204-2 (AWG #20~26, loose piece)
or P/N 170262-2 (AWG #20~26, strip form)
or equivalent

(2) Power interface cable

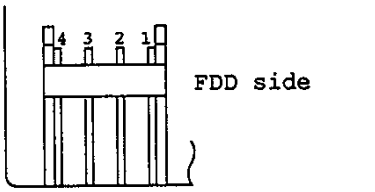
Any appropriate cables taking the maximum power consumption of the FDD will be acceptable.

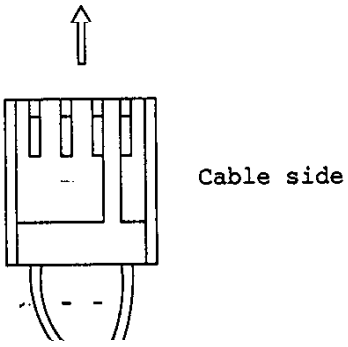
Power voltage	Pin numbers
DC +5V	1
0V	2
(0V)	3
(No connection)	4

(Table 4) Power interface pin-assignment



Rear view





Top view

(Fig.2) Power interface connector external view

8. SIGNAL INTERFACE

8.1 Electrical Characteristics

(1) Interface driver/receiver: See Fig.3.

(2) Electrical characteristics

The following specifications are applicable at the interface connector of the FDD.

(a) Input signal (TTL level)

LOW level (TRUE): 0 ~ 0.7V

Input current: 5.9mA, Max. (including terminator current)

HIGH level (FALSE): 2.2V ~ +5V power voltage

(b) Output signal (Open collector driver)

LOW level (TRUE): 0 ~ 0.4V

Driver sink current capability: 37mA, Max.

HIGH level (FALSE): Depending on host side terminator

(3) Terminator resistor value: 1kΩ ±5%

Terminator (pull-up) resistor is connected to each input signal line (unremovable).

(4) Host side driver: TTL, CMOS, etc.

Required sink current: FDD input current × Number of daisy chained FDD

(5) Host side receiver: TTL, CMOS, etc.

Terminator is required for each output signal line from the FDD.

Host side terminator resistor value: Usually 1 ~ 2.2kΩ is used.

(150Ω , Min.)

8.2 Signal Interface Connector and Cable

(1) Signal interface connector

(a) FDD side connector: Fujitsu, P/N FCN-725P034-AU/O
or equivalent

(b) Pin numbers and pin pitch:
2.54mm (0.1 in) pitch, 34pin block header
(17 pin double rows, even number pins are upper side of the FDD).

(c) Connector external view: See Fig.4.

(d) Connector location: See Fig.1.

(e) Interface connection: See Table 5.

(f) Cable side matched connector:
Fujitsu, P/N FCN-747B034-AU/B (closed end)
or -AU/O (daisy chain) or equivalent.

Note: It is recommended to use a polarizing type connector with a projection on the center of the housing to avoid mis-connection. Refer to Fig.4.
For such a polarizing connector, ∇ mark of the connector housing may show pin No.34.

(2) Signal interface cable

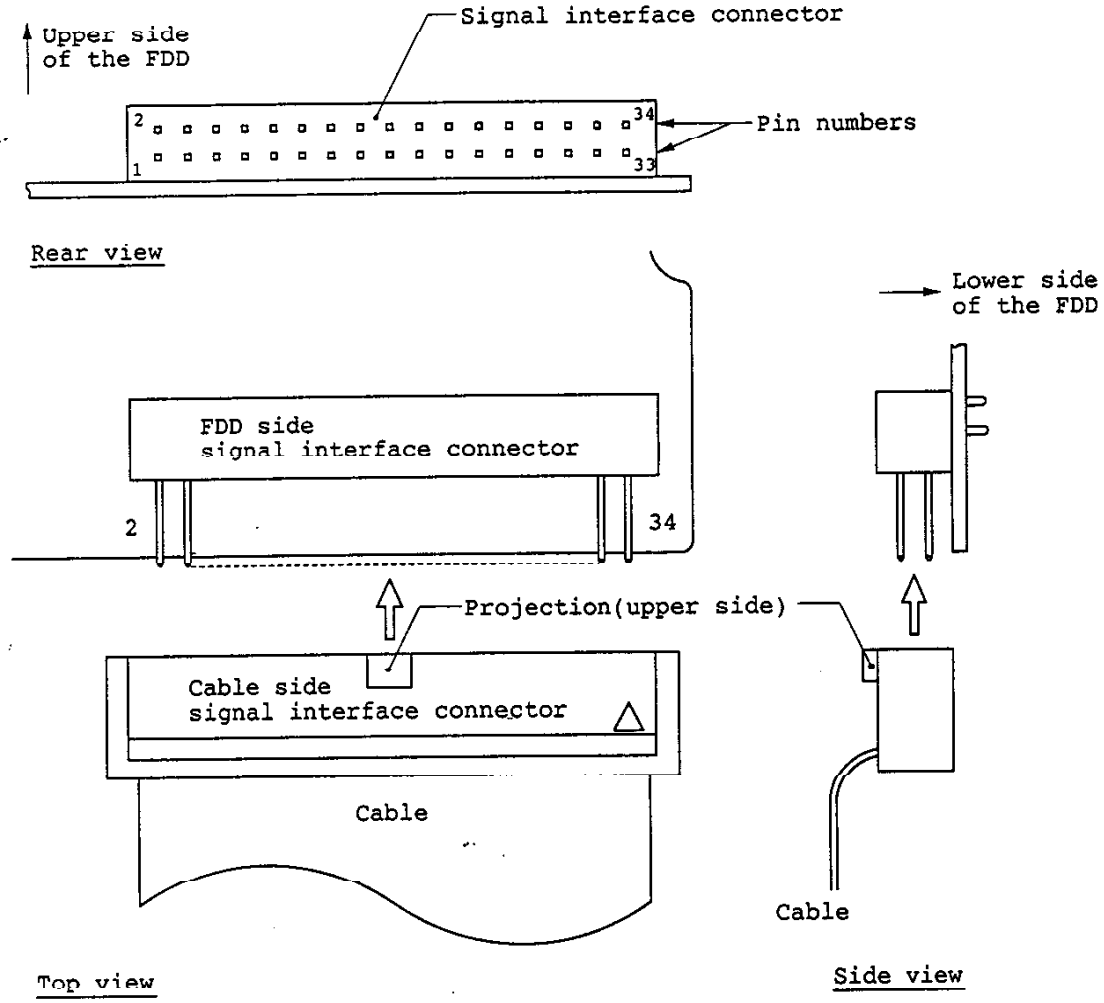
Maximum cable length: 2m (6.6 feet), by terminator of 1kΩ or less
(For daisy chain connection, the total cable length should be less than 2m).
The longer the cable, the smaller the resistor value should be.

Pin Nos.	Signals	Pin Nos.	Signals	Direction
1	NC	2	HD IN/HD OUT/OPEN	In/Out
3	NC	4	NC	-
5	NC	6	NC	-
7	0V	8	INDEX	Output
9	0V	10	DRIVE SELECT 0	Input
11	0V	12	DRIVE SELECT 1	Input
13	0V	14	NC	-
15	0V	16	MOTOR ON	Input
17	0V	18	DIRECTION SELECT	Input
19	0V	20	STEP	Input
21	0V	22	WRITE DATA	Input
23	0V	24	WRITE GATE	Input
25	0V	26	TRACK 00	Output
27	0V	28	WRITE PROTECT	Output
29	0V	30	READ DATA	Output
31	0V	32	SIDE ONE SELECT	Input
33	0V	34	DISK CHANGE	Output

Notes: 1. Refer to item 11 and Table 1 of item 1 as to the signal selection on pin No.2.

2. NC means NO CONNECTION.

(Table 5) Signal interface pin assignment



(Fig.4) Signal interface connector external view

8.3 Input/Output Signals

In the following, input signals are those transmitted to the FDD while output signals are those transmitted from the FDD.
LOW level of the signals is TRUE unless otherwise specified.

8.3.1 DRIVE SELECT 0 and 1 input signals

(1) Signals to select a specific FDD for operation in multiplex control.
(2) Only the DRIVE SELECT signal of the same number as of on-state strap is effective.
(3) All the input/output signals except for the MOTOR ON and HD IN are valid when this signal is effectively received.
(4) The time required to make each input or output signal effective after the transmission of this signal is 0.5μsec, Max. including delay time through the interface cable.
(5) Refer to item 12.1 as to the turn-on condition of the front bezel indicator.
(6) Refer to item 11 as to the strap setting.

8.3.2 MOTOR ON input signal

(1) Level signal to rotate the spindle motor.
(2) The spindle motor reaches to the rated rotational speed within 480msec after this signal changes to TRUE.
(3) Refer to item 12.2 as to the rotational condition of the spindle motor.

8.3.3 DIRECTION SELECT input signal

(1) Level signal to define the moving direction of the head when the STEP line is pulsed.
(2) Step-out (moving away from the center of the disk) is defined as HIGH level of this signal. Conversely, step-in (moving toward the center of the disk) is defined as LOW level of this signal.
(3) The signal shall maintain its level for 0.8μsec, Min. prior to the trailing edge of the STEP pulse. Refer to Fig.10.

8.3.4 STEP input signal

(1) Negative pulse signal to move the head. The pulse width shall be 0.8μ sec or more and the head moves one track space per one pulse.

(2) The access motion (head seek operation) is initiated at the trailing edge of the STEP pulse and completes within 18msec after starting the access including the settling time.

(3) For the subsequent motion in the same direction, the STEP pulses should be input with the interval of 3msec or more, while the pulses should be input with the interval of 4msec or more for a direction change. Refer to Fig.10.
STEP pulses less than 3msec interval for the same direction or less than 4msec interval for a direction change may cause seek error.

(4) STEP pulses are ignored and the access motion is not initiated when one of the following condition is satisfied.
   (a) The WRITE PROTECT signal is FALSE and the WRITE GATE signal is TRUE.
   (b) The TRACK 00 signal is TRUE and the DIRECTION SELECT signal is HIGH level (step-out).
   (c) Step-in operation (DIRECTION SELECT signal is LOW level) from track 81.

8.3.5 WRITE GATE input signal

(1) Level signal to erase the written data and to enable the writing of new data.

(2) The FDD is set to write mode when the following logical expression is satisfied.

$$\text{WRITE GATE} * \text{DRIVE SELECT} * \overline{\text{WRITE PROTECT}}$$

(3) This signal should be made TRUE more than 100μsec after the level change of the SIDE ONE SELECT signal.

(4) The following operations should not be done at least 650μsec (erase delay time) after this signal is changed to FALSE.
   (a) Start the head seek operation by the STEP pulse.
   (b) Change the level of the HD IN signal when the HI strap is on-state.

8.3.6 WRITE DATA input signal

(1) Negative pulse signal to designate the contents of data to be written on a disk. The pulse width should be 0.1μsec through 1.1μsec and the leading edge of the pulse is used.

(2) WRITE DATA pulses are ignored while either of the following condition is satisfied.

(a) The WRITE GATE signal is FALSE.

(b) The WRITE PROTECT signal is TRUE.

(3) This signal should be input according to the timing in Fig.6.
It is recommended to stop the input of the WRITE DATA pulses during the read operation in order to avoid harmful cross talk.

8.3.7 SIDE ONE SELECT input signal

(1) Level signal to designate which side of a double sided disk is used for reading or writing.

(2) When this signal is HIGH level, the magnetic head on the side 0 surface (lower side) of the disk is selected, while the magnetic head on the side 1 surface (upper side) is selected when this signal is LOW level.

(3) The READ DATA pulse on a selected surface is valid more than 100μsec after the change of this signal level.

(4) Write operation (the WRITE GATE signal is TRUE) on a selected surface shall be started more than 100μsec after the change of this signal level.

8.3.8 TRACK 00 output signal

(1) Level signal to indicate that the head is on track 00.
(2) This signal is valid more than 2.8msec, after the effective receival of the STEP pulse.

8.3.9 INDEX output signal

(1) Negative pulse signal to indicate the start point of a track and one index pulse per one disk revolution is output.
(2) INDEX pulse is output when the following logical expression is satisfied.

Index detection * DRIVE SELECT * Ready state * Seek-complete

Notes: (a) Ready state is the Anded condition of power-on, disk installed, auto-chucking completed, 484 ~ 505msec passed after motor-on command, and INDEX pulse detected.
(b) Seek-complete means the state that 15.8 ~ 17.9msec has been passed after the trailing edge of the final STEP pulse.

(3) Fig.5 shows the timing of this signal. Pulse width is 1.5msec through 5msec and the leading edge of the pulse shall be used as the reference.

8.3.10 READ DATA output signal

(1) Negative pulse signal for the read data from a disk composing clock bits and data bits together.
(2) Fig.7 shows the timing of this signal. Pulse width is 0.15μsec through 0.8μsec and the leading edge of the pulse shall be used as the reference.
(3) READ DATA pulse is output when the following logical expression is satisfied.

Read data detection * DRIVE SELECT * $\overline{\text{Write operation}}$ * Ready state * Seek-complete

Notes: (a) Refer to item 8.3.9 (2) as to the ready state.
(b) $\overline{\text{Write operation}}$ is the state while the WRITE GATE input signal is FALSE and erase delay time has been passed after the WRITE

GATE signal changed to FALSE.

(c) Refer to item 8.3.9 (2) as to the seek-complete.

(4) Output pulses are invalid while one of the following condition is not satisfied.

(a) 100μsec has been passed after the level change of the SIDE ONE SELECT signal.

(b) 650μsec (2MB mode) or 690μsec (1MB mode) has been passed after the WRITE GATE signal is changed to FALSE.

8.3.11 WRITE PROTECT output signal

(1) Level signal to indicate that the write inhibit hole of an installed disk is open.

(2) When this signal is TRUE, data on the disk are protected from miserasing and write operation is inhibited.

8.3.12 DISK CHANGE output signal

(1) Level signal to indicate that a disk in the FDD is ejected.

(2) This signal changes to TRUE when either of the following condition is satisfied.

(a) Power on.

(b) A disk is removed.

(3) The signal returns to FALSE when both of the following conditions are satisfied. Refer to Fig.8.

(a) A disk has been installed.

(b) A STEP command is received when the DRIVE SELECT signal is TRUE.

8.3.13 Input/Output signals for density mode setting by the HA/HI/HO straps

There are three basic methods for setting the density mode of the FDD as shown in the following. Refer to item 11 as to the setting of the HA/HI/HO straps.

8.3.13.1 Method 1 using HD IN input signal (HI strap on)

(1) HIGH or LOW level of the HD IN signal from host controller is used to designate the density mode of the FDD. There is no output signal from the FDD for disk type identification.

(2) One of the following level assignments can be selected by the LHI strap.

(a) LHI strap is off:

When the HD IN signal is HIGH level, the FDD is set to the 2MB mode, while it is set to the 1MB mode when the signal is LOW level.

(b) LHI strap is on:

When the HD IN signal is LOW level, the FDD is set to the 2MB mode, while it is set to the 1MB mode when the signal is HIGH level.

8.3.13.2 Method 2 without using any interface signal (HA strap on)

(1) Interface signal is not used between the FDD and host controller (signal interface pin No.2 is OPEN). Density modes of the FDD and host system are determined independently.

(2) The density mode of the FDD is automatically set by discriminating the HD hole of an installed disk. If the density mode of the FDD is not coincident with that of the host controller, data errors always occur at read operation.

8.3.13.3 Method 3 using HD OUT output signal (HO strap on)

(1) The density mode of the FDD is automatically set by discriminating the HD hole of an installed disk.

(2) HIGH or LOW level of the HD OUT signal from the FDD is used to inform host controller which type of disk is installed in the FDD. And the density mode of the host is automatically determined according to this signal.

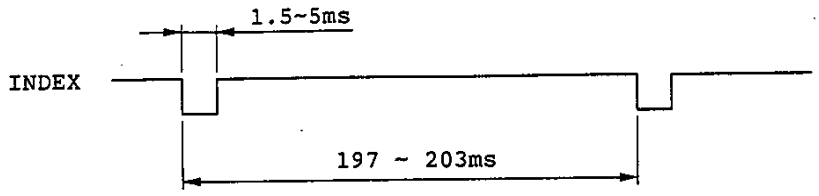
(3) The HIGH level of the HD OUT signal means that a 2HD (high density) disk is installed or no disk is installed in the FDD, while a 2DD (normal density) disk is installed at the LOW level of this signal.

8.3.14 NO CONNECTION (NC)

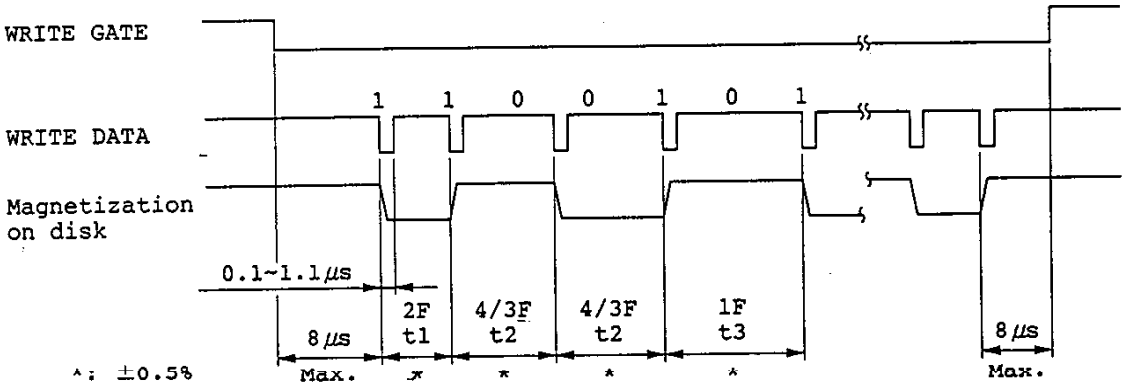
The NC pins are electrically isolated from any other circuit in the FDD.

8.3.15 Treatment of not-used signals

If some of the provided input/output signals are not necessary for your application, keep off the FDD straps for the unused signals referring to item 11, or keep the unused signal lines open or connect appropriate pull-up resistor (more than 150Ω) at the host side.

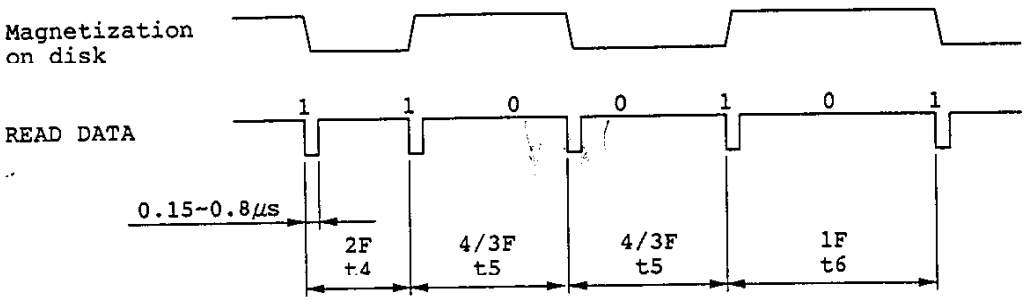


(Fig.5) INDEX timing



Density mode	rpm	t1	t2	t3
2MB	300	2μs, Nom.	3μs, Nom.	4μs, Nom.
1MB	300	4μs, Nom.	6μs, Nom.	8μs, Nom.

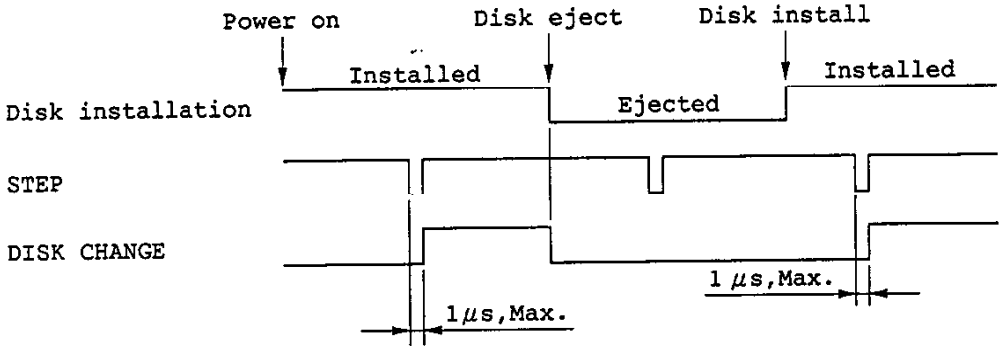
(Fig.6) WRITE DATA timing (MFM method)



Note: READ DATA pulse will be detected within t7 from its nominal position.
(When PLO separator is used with recommended write pre-compensation.)

Density mode	rpm	t4	t5	t6	t7
2MB	300	2μs, Nom.	3μs, Nom.	4μs, Nom.	±350ns
1MB	300	4μs, Nom.	6μs, Nom.	8μs, Nom.	±700ns

(Fig.7) READ DATA timing (MFM method)



Note: To simplify the timing chart, the DRIVE SELECT signal is assumed always TRUE in the above figure.

(Fig.8) DISK CHANGE signal timing

9. CONTROL SEQUENCE

9.1 Power-on

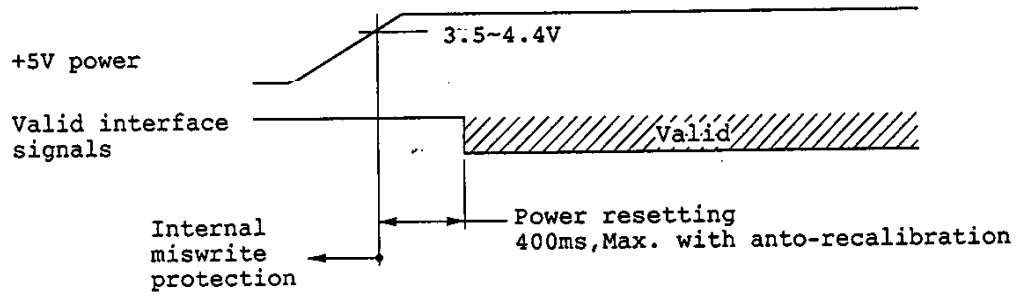
(1) Rise and fall time of +5V power: Not specified.

(2) Protection against power on and off

(a) In the transient period when the +5V power is lower than 3.5V, the FDD is protected against miswriting and miserasing whatever the state of input signals are.

(b) Except for the condition of item (a), the FDD is protected against miswriting and miserasing as long as the WRITE GATE input signal does not change to TRUE.

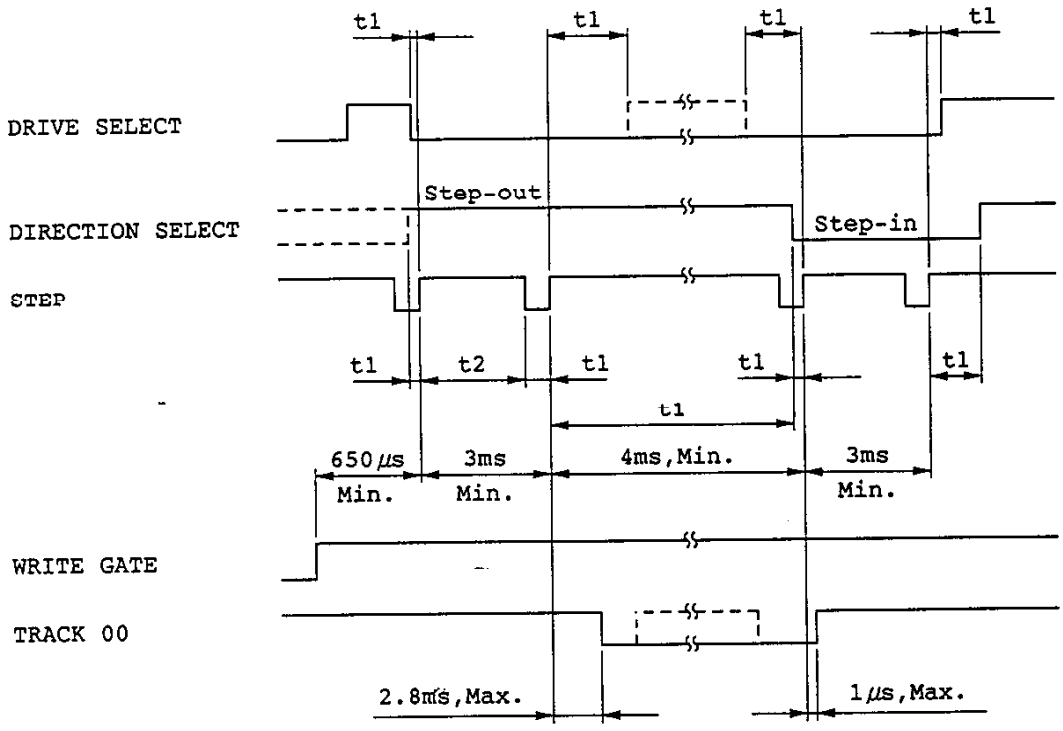
(3) Power reset time in FDD: Less than 400msec, including auto-recalibration



(Fig.9) Power on sequence

9.2 Seek Operation

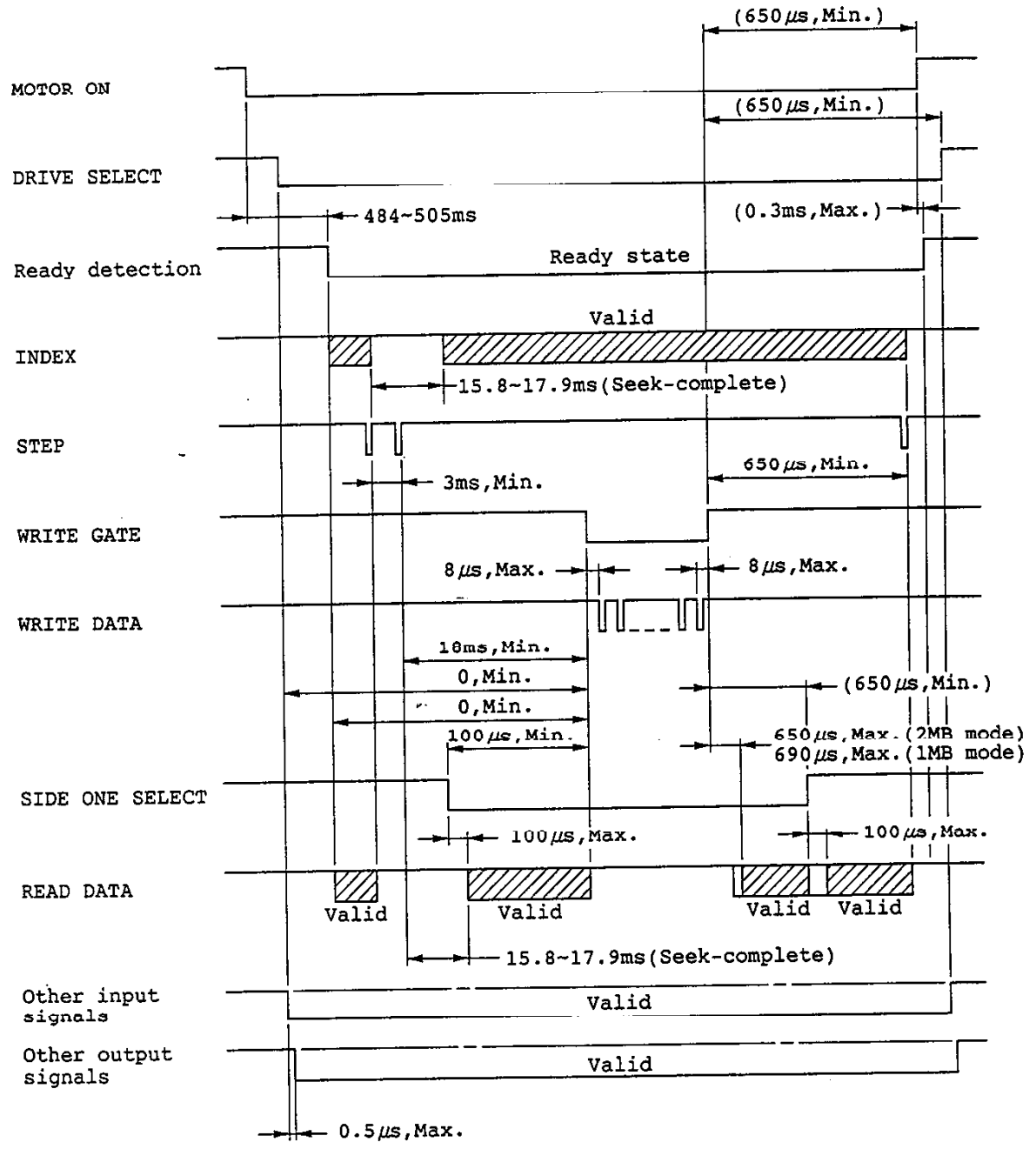
Seek operation can be done independently of the spindle motor rotation.



$t1 \geqq 0.8\,\mu s$ $t2 \geqq 2\,\mu s$

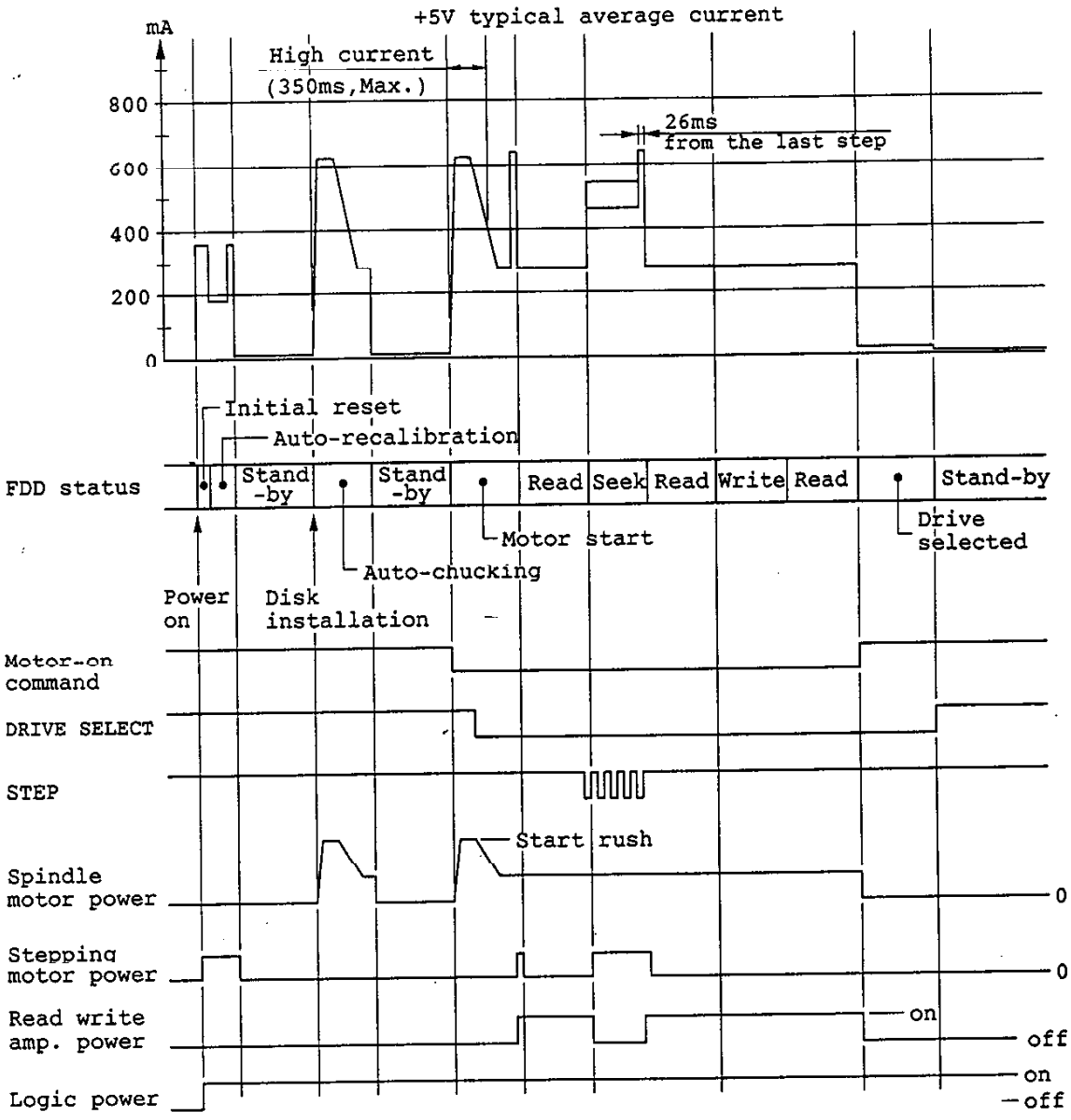
(Fig.10) Seek operation timing

9.3 Read Write Operation



(Fig.11) Read/Write operation timing

9.4 Current Consumption Profile



(Fig.12) Typical average current profile

(1) Stand-by mode

When both of the following conditions are satisfied, FDD goes to the stand-by mode (low power consumption mode).

(a) The spindle motor stops.
(b) Not in the seek-operation (including the settling time).

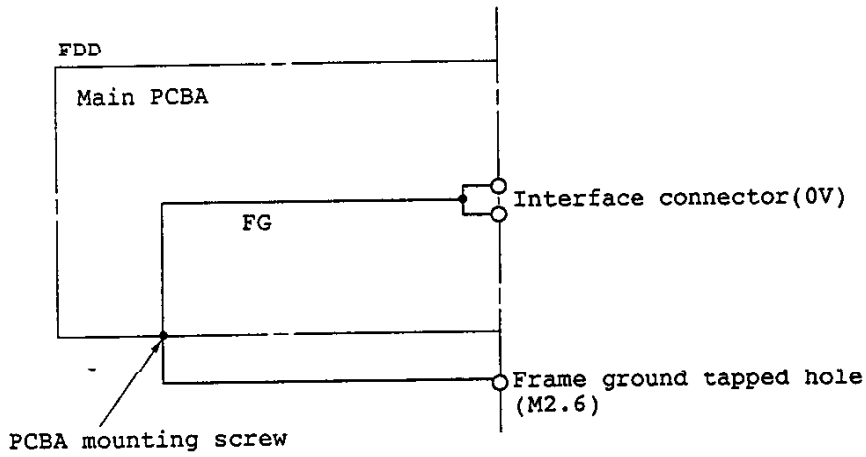
Note: In the stand-by mode, the FDD can immediately respond to a command from host controller with no restriction.
If the polling operation of the DRIVE SELECT line is done in the stand-by mode, current flows intermittently and +5V current slightly increases.

(2) Simultaneous operation of motor start and seek

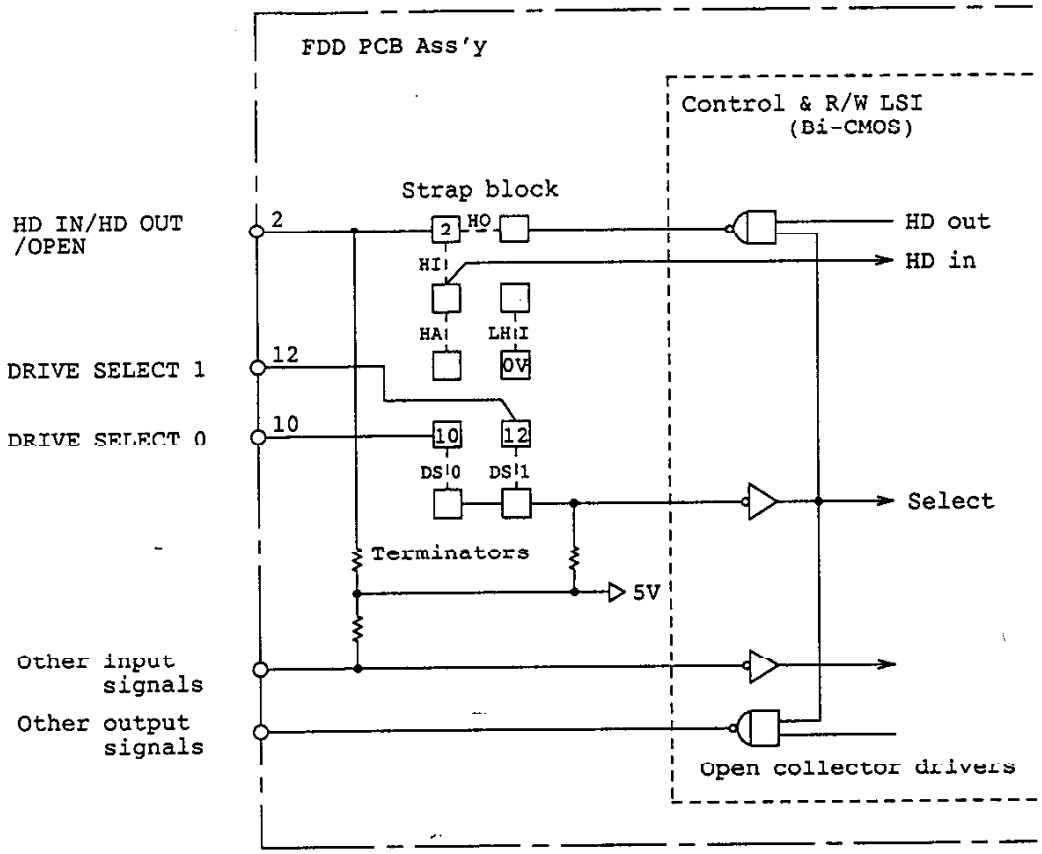
If a seek operation is done during the start-up of the spindle motor, or if the motor starts during the seek operation, +5V current at motor start increases by 0.38A, Max. from the value in Table 3. Stepping motor is energized at high power from the first STEP to 26msec after the last STEP.

10. FRAME GROUNDING

The FDD frame is electrically connected to DC 0V by the mounting screw of the main PCBA. (See Fig.13).



(Fig.13) Frame ground internal connection



(Fig.3) FDD signal interface circuit

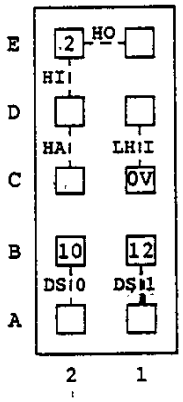
11. CUSTOMER SELECTABLE STRAPS

11.1 Function Summary of Straps

The FDD is equipped with the following selectable straps on the main PCBA. Insertion of a short bar onto the post pin is defined as the on-state of the strap. Refer to Table 1 in item 1 as to the strap setting at delivery.

Strap	Function
DS0	DRIVE SELECT 0 input on pin 10
DS1	DRIVE SELECT 1 input on pin 12
HA	Density set automatically (Method 2)
HI	Density set by HD IN on pin 2 (Method 1)
HO	HD OUT on pin 2 (Method 3)

Note: Refer to item 8.3.13 as to the details of the methods 1 ~ 3 for density mode setting.



Strap-post layout

(Table 6) Function summary of straps

11.2 DS0 and DS1 Straps

(1) In the multiplex control, these straps designate the address of the FDD.
(2) By the combination with the DRIVE SELECT 0 and 1 signals, two addresses, can be designated. Refer to Fig.3 and Table 6.

11.3 HA/HI/HO Straps

(1) Straps to select a designating method of the density mode. Refer to item 8.3.13.
(2) Table 7 shows the combination of the straps and selectable functions.
(3) Refer to item 11.4 as to the LHI strap.

Method	Strap setting				Pin 2 Function	HD level	Density designation	
	HA	HI	HO	LHI			Host side	FDD side
1A	-	ON	-	-	HD IN	HIGH	Key-in or software	HD IN from host
1B	-	ON	-	ON	HD IN	LOW		
2	ON	-	-	-	OPEN	-	Key-in or software	Automatic by sensor
3	ON	-	ON	-	HD OUT	HIGH	HD OUT from FDD	Automatic by sensor

Notes: 1. "-" mark indicates the off-state of the strap.
2. LHI strap must be off-state except for the method 1B.
3. "HD level" means the level of the HD IN or HD OUT signal for 2MB mode.

(Table 7) Designating method for density mode

11.4 LHI Strap

(1) Strap to change the level meaning of the HD IN signal.
(2) This strap is effective only when the HI strap is on-state. When the HI strap is off-state, the LHI strap must be also off-state.
(3) Refer to item 8.3.13.1 or Table 7 as to the level meaning of the HD IN signal.

12. TURN ON CONDITION OF INDICATOR AND SPINDLE MOTOR

12.1 Front Bezel Indicator

The indicator (LED) turns-on while the DRIVE SELECT signal is TRUE. However, the indicator keeps off until 3.1msec has passed after the DRIVE SELECTion to avoid the polling operation of the DRIVE SELECT signal.

12.2 Spindle Motor

(1) The spindle motor rotates while the MOTOR ON signal is TRUE. However, the spindle motor does not rotate at any condition while no disk is installed.

(2) Auto-chucking operation is executed at each disk installation by rotating the spindle motor for 490msec, approx. (500msec, Max.). All the interface signals are valid according to the explanation in item 8.3 while the auto-chucking operation is in progress.